WHAT IS CLAIMED IS:

1. A reliability evaluation test apparatus which tests a reliability of a semiconductor wafer on the basis of a test signal from a measurement unit, comprising a measurement section and a storage section which has a hermetic and heat insulating structure, stores a semiconductor wafer that is totally in electrical contact with a contactor, and transmits/receives a test signal to/from the measurement section, comprising:

a pressure mechanism which presses the contactor in the storage section; and

a heating mechanism which heats the semiconductor wafer that is totally brought into contact with the contactor by the pressure mechanism to a predetermined temperature,

wherein the reliability evaluation test apparatus evaluates reliability of a multilayered interconnection and an insulting film, which are formed on the semiconductor wafer, under an accelerated condition.

2. A reliability evaluation test apparatus according to claim 1, wherein the storage section has a table which has a heat insulating structure and on which the semiconductor wafer is placed, a connection ring which surrounds the table and comes into electrical contact with the contactor, and a wiring board which comes into electrical contact with the

connection ring and transmits/receives the test signal to/from the measurement section.

3. A reliability evaluation test apparatus according to claim 2, further comprising, on the connection ring, a seal member which comes into contact with the contactor to seal a space in the storage section from an outside, and means for supplying an inert gas and/or reducing gas into the storage section.

4. A reliability evaluation test apparatus according to claim 1, wherein the pressure mechanism comprises a pressure plate which presses the contactor, a bellows whose lower end is connected to the pressure plate, a support which is connected to an upper end of the bellows and can move vertically, and means for supplying a gas into a space formed by the pressure plate, the bellows, and the support.

5. A reliability evaluation test apparatus according to claim 1, wherein the heating mechanism comprises a heater which uniformly heats an entire surface of the semiconductor wafer from a lower surface side and also serves as the table.

6. A reliability evaluation test apparatus according to claim 5, wherein the heater comprises a first heater which heats a central portion of the semiconductor wafer, and a second heater which surrounds the first heater and heats an outer edge portion of the semiconductor wafer.

7. A reliability evaluation test apparatus according to claim 5, wherein the heating mechanism comprises an auxiliary heater which heats the entire surface of the semiconductor wafer from an upper surface side.

8. A reliability evaluation test apparatus according to claim 1, wherein the measurement section comprises an electromigration measurement section and a leakage current measurement section.

9. A reliability evaluation test apparatus according to claim 8, further comprises a switching mechanism which alternately switches between the measurement sections.

10. A reliability evaluation test apparatus according to claim 8, wherein the electromigration measurement section comprises a function of supplying three kinds of currents including a DC current, a pulse DC current, and an AC current.

11. A reliability evaluation test apparatus according to claim 1, in which a plurality of test patterns 77 are formed on the semiconductor wafer, and which comprises a test pattern grouping function of putting the plurality of test patterns into groups and executing a reliability evaluation test for not less than five groups simultaneously.

12. A reliability evaluation test apparatus according to claim 1, further comprising an anisotropic

conductive film between the contactor and the semiconductor wafer.

13. A reliability evaluation test apparatus according to claim 1, wherein the measurement section simultaneously executes a reliability evaluation test of not less than 100 semiconductor devices formed on the semiconductor wafer.

14. A reliability evaluation test apparatus according to claim 1, wherein the storage section comprises a heat insulating structure which maintains the semiconductor wafer at a temperature of not less than 160°C.

15. A reliability evaluation test apparatus according to claim 1, wherein the contactor includes a heat-resistant substrate, and a thermal expansion coefficient of the heat-resistant substrate is 1 to 50 ppm/°C.

16. A reliability evaluation test system comprising: an aligner which totally brings a contactor into contact with a semiconductor wafer; a transfer tool which transfers the contactor and the semiconductor wafer, which are totally kept in contact with each other by the aligner; and a reliability evaluation test apparatus of claim 1, which executes a reliability evaluation test of the semiconductor wafer transferred by the transfer tool.

17. A reliability evaluation test system according

to claim 16, which allows data communication between the aligner and the reliability evaluation test apparatus.

18. A reliability evaluation test system according to claim 16, wherein the aligner includes a microscope to observe the semiconductor wafer on the basis of a test result of the semiconductor wafer.

19. A reliability evaluation test system according to claim 16, wherein the transfer tool includes a magnet to integrate the contactor and the semiconductor wafer.

20. A reliability evaluation test system according to claim 16, wherein the transfer tool includes a magnetic circuit and switch means for turning on/off the magnetic circuit, and the switch means excites/degausses the magnetic circuit to cause the transfer tool to attract/release the contactor and the semiconductor wafer.

21. A contactor, which comprises a heat-resistant substrate having a thermal expansion coefficient of 1 to 50 ppm/°C, and a conductor circuit formed on the heat-resistant substrate, and is used to execute a reliability evaluation test at a temperature of not less than 160°C.

22. A contactor according to claim 21, wherein the conductor circuit comprises a bump.

23. A contactor according to claim 21, wherein the

heat-resistant substrate is formed from at least one material selected from a heat-resistant resin, a metal, a semiconductor, and a ceramic.

24. A contactor according to claim 21, wherein an insulating coating is formed on a surface except a portion which is electrically connected in executing the reliability evaluation test.

25. A reliability evaluation test method of executing different reliability evaluation tests for a semiconductor wafer in a state wherein the semiconductor wafer and a contactor are totally in electrical contact with each other.

26. A reliability evaluation test method of executing a reliability evaluation test for a semiconductor wafer by pressing the semiconductor wafer and a contactor which are totally in electrical contact with each other, heating the semiconductor wafer to not less than 160°C, and rendering the semiconductor wafer conductive.

27. A reliability evaluation test method according to claim 25, wherein the reliability evaluation test is executed simultaneously for not less than 100 semiconductor devices on the semiconductor wafer.

28. A reliability evaluation test method according to claim 25, wherein an electromigration test and/or a leakage current test is executed as the reliability evaluation test.

29. A reliability evaluation test method according to claim 25, wherein a temperature distribution in a surface of the semiconductor wafer is controlled within ±2.0°C at a range of 160°C to 350°C.

30. A reliability evaluation test method according to claim 25, wherein the semiconductor wafer and the contactor are placed in one of an inert gas atmosphere and an atmosphere of an inert gas mixed with a reducing gas.

31. A reliability evaluation test method according to claim 30, wherein an oxygen concentration in the atmosphere is not more than 100 ppm.